Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (original) A method for generating an error signal, comprising the steps of:

accumulating sign information relating to phase differences in received signals;

comparing the accumulated sign information against predetermined threshold levels; and

generating the error signal when at least one of the predetermined threshold levels is satisfied.

2. (original) The method according to claim 1 wherein the error signal is generated in an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system.

3. (original) The method according to claim 2, further comprising the steps of:

multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal; and

obtaining a sign value of a product of said multiplying step.

4. (original) The method according to claim 3, wherein said step of obtaining a sign value comprises the step of extracting the sign value of an imaginary part of the product of said multiplying step.

5. (original) The method according to claim 1, wherein said predetermined threshold levels include a positive threshold and a negative threshold.

6. (original) The method according to claim 5, wherein said generating step comprises the steps of generating a positive constant error signal when the positive threshold is satisfied, and generating a negative constant error signal when the negative threshold level is satisfied.

7. (original) The method according to claim 6, wherein the positive constant error signal and the negative constant error signal are used to control a gain of an AFC loop.

8. (original) The method according to claim 1, further comprising the step of utilizing values of the error signal to control a gain in an AFC loop.

9. (original) The method according to claim 8, wherein the values of the error signals are constant values capable of being adjusted to control the gain in the AFC loop.

10. (original) The method according to claim 1, further comprising the step of utilizing the predetermined threshold levels to affect a bandwidth of an AFC loop.

11. (original) The method according to claim 1, further comprising the step of resetting the accumulated sign information when the error signal is generated.

12. (original) A method for generating an error signal for an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system, comprising the steps of:

accumulating sign information relating to phase differences in received pilot signals;

decimating the accumulated sign information; and

utilizing an output of said decimating step as the error signal for the AFC loop.

13. (original) The method according to claim 12, further comprising the steps of:

multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal; and

obtaining a sign value of a product of said multiplying step.

14. (original) The method according to claim 13, wherein said step of obtaining the sign value comprises the step of extracting the sign value of an imaginary part of the product of said multiplying step.

15. (original) The method according to claim 12, wherein the output of said decimating step is utilized as the loop error signal upon a decimation of a threshold number of the samples.

16. (original) The method according to claim 15, further comprising the step of resetting the output of said decimating step at a same interval as when the output of said decimating step is utilized as the loop error signal.

17. (original) An apparatus for generating an error signal, comprising:

an accumulator for accumulating sign information relating to phase differences in received pilot signals;

a comparator for thresholding the accumulated sign information against adaptable threshold levels; and

an error signal generator for generating the error signal when at least one of the adaptable threshold levels is satisfied.

18. (original) The apparatus according to claim 17, wherein said error signal generator generates a positive constant error signal when the positive threshold is satisfied, and generates a negative constant error signal when the negative threshold level is satisfied.

19. (original) The apparatus according to claim 18, wherein the positive constant error signal and the negative constant error signal are used to control a gain of an AFC loop.

20. (original) An apparatus for generating an error signal for an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system, comprising:

an accumulator for accumulating sign information relating to phase differences in received pilot signals;

a decimator for decimating the accumulated sign information so as to output the error signal therefrom.

21. (original) The apparatus according to claim 20, wherein the output of said decimator is utilized as the error signal upon a decimation of a threshold number of the samples.

22. (original) The apparatus according to claim 21, wherein the output of said decimator is reset at a same interval as when the output of said decimator is utilized as the error signal.

23. (new) A method for generating a loop error signal for a delay-lock code tracking loop in a CDMA system, comprising the steps of:

accumulating sign information relating to phase differences between samples of a received code sequence;

comparing the accumulated sign information against adaptable threshold levels; and

generating the loop error signal when at least one of the adaptable threshold levels is satisfied.

24. (new) The method according to claim 23, further comprising the steps of:

calculating a first integral corresponding to products of some of the samples and a scrambling code sequence;

calculating a second integral corresponding to products of later occurring ones of the samples and the scrambling code; and

subtracting the second integral from the first integral to obtain the sign information.

25. (new) The method according to claim 24, wherein each of the first integral and the second integral are calculated over a code tracking dwell time.

26. (new) The method according to claim 23, wherein said accumulating step accumulates the sign information from a sample error signal $e[m]$, wherein $e[m]$ is equal to

$$\sum_{n=0}^{N_D-1} R_E[mN_D+n]Sc[mN_D+n] - \sum_{n=0}^{N_D-1} R_L[mN_D+n]Sc[mN_D+n]$$

wherein R_E and R_L respectively represent earlier occurring samples and later occurring samples with respect to on-time occurring samples, n is an index of the samples in a chip rate, N_D is a code tracking dwell time, Sc is a local scrambling code sequence, and m is an index of the sample error signal $e[m]$.

27. (new) The method according to claim 23, wherein the adaptable threshold levels include a positive threshold and a negative threshold.

28. (new) The method according to claim 27, wherein said generating step comprises the step of generating a positive constant loop error signal when the positive threshold is satisfied, and generating a negative constant loop error signal when the negative threshold level is satisfied.

29. (new) The method according to claim 28, wherein the positive constant loop error signal and the negative constant loop error signal are used to control a gain of the delay-lock code tracking loop.

30. (new) The method according to claim 23, further comprising the step of utilizing values of the loop error signal to control a gain in the delay-lock code tracking loop.

31. (new) The method according to claim 30, wherein the values of the loop error signal are constant values capable of being adjusted to control the gain in the delay-lock code tracking loop.

32. (new) The method according to claim 23, further comprising the step of utilizing the adaptable threshold levels to affect a bandwidth of the delay-lock code tracking loop.

33. (new) The method according to claim 23, wherein the delay-lock code tracking loop includes a receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

34. (new) The method according to claim 33, further comprising the step of filtering the loop error signal prior to said adjusting step.

35. (new) An apparatus for generating an error signal for a delay-lock code tracking loop in a CDMA system, comprising:

an accumulator for accumulating sign information relating to phase differences between samples of a received code sequence;

a comparator for comparing the accumulated sign information against adaptable threshold levels; and

an error signal generator for generating the error signal when at least one of the adaptable threshold levels is satisfied.

36. (new) The apparatus according to claim 35, further comprising an arithmetic module for calculating a first integral corresponding to products of some of the samples and a scrambling code sequence, calculating a second integral corresponding to products of later occurring ones of the samples and the scrambling code, and subtracting the second integral from the first integral.

37. (new) The apparatus according to claim 36, wherein each of the first integral and the second integral are calculated over a code tracking dwell time.

38. (new) The apparatus according to claim 35, wherein said accumulator is for accumulating the sign information from a sample error signal $e[m]$, wherein $e[m]$ is equal to

$$\sum_{n=0}^{N_D-1} R_E[mN_D+n]Sc[mN_D+n] - \sum_{n=0}^{N_D-1} R_L[mN_D+n]Sc[mN_D+n]$$

wherein R_E and R_L respectively represent earlier occurring samples and later occurring samples with respect to on-time occurring samples, n is an index of the samples in a chip rate, N_D is a code tracking dwell time, Sc is a local scrambling code sequence, and m is an index for the sample error signal $e[m]$.

39. (new) The apparatus according to claim 35, wherein said error signal generator is for generating a positive constant error signal when a positive threshold is satisfied, and generates a negative constant error signal when a negative threshold level is satisfied.

40. (new) The apparatus according to claim 39, wherein the positive constant error signal and the negative constant error signal are for controlling a gain of the delay-lock code tracking loop.

41. (new) The apparatus according to claim 35, further comprising a receiver sample buffer for allowing the samples of the received code sequence to be retrieved there from with different delays, and for adjusting positions of the samples in the buffer based on the error signal.

42. (new) The apparatus according to claim 41, further comprising a filter for filtering the error signal prior to adjusting the positions of the samples in the receiver sample buffer.

43. (new) A method for generating a loop error signal for a delay-lock code tracking loop in a CDMA system, comprising the steps of:

accumulating sign information relating to phase differences between samples of a received code sequence;

decimating the accumulated sign information; and

utilizing an output of said decimating step as the loop error signal for the delay-lock code tracking loop.

44. (new) The method according to claim 43, wherein the output of said decimating step is utilized as the loop error signal upon a decimation of a threshold number of the samples.

45. (new) The method according to claim 44, further comprising the step of resetting the output of said decimating step at a same interval as when the output of said decimating step is utilized as the loop error signal.

46. (new) The method according to claim 43, further comprising the steps of:

calculating a first integral corresponding to products of some of the samples and a scrambling code sequence;

calculating a second integral corresponding to products of later occurring ones of the samples and the scrambling code; and

subtracting the second integral from the first integral to obtain the sign information.

47. (new) The method according to claim 46, wherein each of the first integral and the second integral are calculated over a code tracking dwell time.

48. (new) The method according to claim 43, wherein said accumulating step accumulates the sign information from a sample error signal $e[m]$, wherein $e[m]$ is equal to

$$\sum_{n=0}^{N_D-1} R_E[mN_D+n]Sc[mN_D+n] - \sum_{n=0}^{N_D-1} R_L[mN_D+n]Sc[mN_D+n]$$

wherein R_E and R_L respectively represent earlier occurring samples and later occurring samples with respect to on-time occurring samples, n is an index of the samples in a chip rate, N_D is a code tracking dwell time, Sc is a local scrambling code sequence, and m is an index for the sample error signal $e[m]$.

49. (new) The method according to claim 43, wherein the delay-lock code tracking loop includes a receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

50. (new) The method according to claim 43, further comprising the step of filtering the loop error signal prior to said adjusting step.

51. (new) An apparatus for generating a loop error signal for a delay-lock code tracking loop in a CDMA system, comprising:

an accumulator for accumulating sign information relating to phase differences between samples of a received code sequence; and

a decimator for receiving the accumulated sign information from said accumulator and for decimating the accumulated sign information,

wherein an output of said decimator is utilized as the loop error signal for the delay-lock code tracking loop.

52. (new) The apparatus according to claim 51, wherein the output of said decimator is utilized as the loop error signal upon a decimation of a threshold number of the samples.

53. (new) The apparatus according to claim 52, wherein the output of said decimator is reset at a same interval as when the output of said decimator is utilized as the loop error signal.

54. (new) The apparatus according to claim 51, further comprising an arithmetic module for calculating a first integral corresponding to products of some of the samples and a scrambling code sequence, calculating a second integral corresponding to products of later occurring ones of the samples and the scrambling code, and subtracting the second integral from the first integral.

55. (new) The apparatus according to claim 54, wherein each of the first integral and the second integral are calculated over a code tracking dwell time.

56. (new) The apparatus according to claim 51, wherein said accumulator is for accumulating the sign information from a sample error signal $e[m]$, wherein $e[m]$ is equal to

$$\sum_{n=0}^{N_D-1} R_E[mN_D+n]Sc[mN_D+n] - \sum_{n=0}^{N_D-1} R_L[mN_D+n]Sc[mN_D+n]$$

wherein R_E and R_L respectively represent earlier occurring samples and later occurring samples with respect to on-time occurring samples, n is an index of the samples in a chip rate, N_D is a code tracking dwell time, Sc is a local scrambling code sequence, and m is an index for the sample error signal $e[m]$.

57. (new) The apparatus according to claim 51, further comprising a receiver sample buffer for allowing the samples of the received code sequence to be retrieved there from with different delays, and for adjusting positions of the samples in the buffer based on the error signal.

58. (new) The apparatus according to claim 57, further comprising a filter for filtering the error signal prior to adjusting the positions of the samples in the receiver sample buffer.